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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/651,310	08/30/2000	Shunpei Yamazaki	07977/151002/US3339D1	2287

7590 10/27/2004

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EXAMINER	
PARKER, KENNETH	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 10/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/651,310	YAMAZAKI, SHUNPEI	
	Examiner	Art Unit	
	Kenneth A Parker	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10,11,15,19,22-34,36 and 37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10,11,15,19,22-34,36 and 37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obvious to one of ordinary skill ness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to one of ordinary skill at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims1, 3-5, 8, 10, 15, 22, 24-30, 31-32, are rejected under 35 U.S.C. 103(a) as being unpatentable over Misawa 5250931 in view of Lebrun et al 5606194, Adachi et al, 5155612, Kondo 5625473 and Nishiguchi et al 5621553.

Claim 1 is written to A display device comprising: a pair of substrates;an active matrix circuit and peripheral driver circuit provided on one of the pair of the substrates; and a sealing member formed substrates so to seal the peripheral driver circuit, with sealing member being capable light blocking wherein said sealing member comprises a **pigment for light blocking**. Claim 8 is an electronic device comprising: first substrate and a second substrate; a driver circuit region formed on said first substrate, said diver circuit region having at least one of a register circuit, NAND circuit, level shifter circuit and a buffer circuit; an active matrix region formed on said first substrate, said active matrix region having at least a pixel; a sealing member formed between said first and second substrates, said sealing member bonding said first and second substrates and covering said driver circuit region; wherein said sealing member

shields said wherein said sealing member comprises **a pigment for light blocking.** Clam 16 is a display device comprising: at least a first substrate and a second substrate; formed on said first a driver circuit region substrate, said diver circuit region having at least a register circuit, a NAND circuit, a level shifter circuit, **OR** a buffer circuit, wherein at least a CMOS transistor is formed in driver circuit region, CMOS thin film transistor and a first n-channel p-channel thin film transistor; an active matrix region formed said first substrate, said active matrix region having at least a pixel, wherein a second p-channel film transistor formed in said pixel; a sealing member formed between said first and second substrates and covering said driver circuit region; and sealing member bonding said first and second wherein **said sealing member comprises pigment light blocking and wherein said sealing member shields said driver circuit region from light.**

Misawa discloses a liquid crystal device with P and N type cmos transistors in the driver circuits which include a buffer, and P or N drivers in the active region. The device includes the use as a projectior, and is not shown with a black matrix. Lacking is the sealant over the circuit with a pigment for blocking light. Lebrun et al teaches that using a sealant over the circuit (figure 1) enables the low cost protection, and having the sealant be opaque gives the added benefit of protecting the circuit from light. Therefore it would have been obvious to one of ordinary skill , in the device of Misawa, to employ an opaque seal for enclosing the liquid crystal and bonding the substrate to cover the circuit for the low cost protection form the enviroment and light. Still lacking is the use of a pigment.

Adachi et al teaches that the sealants need to be able to block light, and adds pigments to the dyes to assure sufficient light blocking (col. 7, lines 16-20). Therefore it would have been obvious to one of ordinary skill , in the device of Hayashi, to use a light blocking sealant with coloring agents (pigment), to ensure sufficient light blocking as taught by Adachi et al. Many of the low cost conventional sealants, such as polyimide and acrylic require pigment pigments to block light. Therefore, it would have been obvious to one of ordinary skill to employ pigments in order to enable use of the conventional low cost materials.

The rejection can be viewed as Lebrun in view of Misawa and the two secondary references Adachi and Castleberry, both provided to show the well known nature of the use of dyes for creating light blocking sealants. Misawa teaches that their CMOS active matrix and drivers enables low cost with a high reliability and resolution (column 2, lines 38-40). Therefore, it would have been obvious to one of ordinary skill , in the device of Lebrun, to employ the CMOS active matrix and driver structure of Misawa for the benefits of low cost with a high reliability and resolution. This teaching of Misawa was, at the time of invention, notoriously well known, and would have been further obvious to one of ordinary skill for that reason. For this version, still lacking is the use of a pigment. Adachi et al teaches that the sealants need to be able to block light, and adds pigments to the dyes to assure sufficient light blocking (col. 7, lines 16-20). Therefore it would have been obvious to one of ordinary skill , in the device of Hayashi, to use a light blocking sealant with coloring agents (pigment), to ensure sufficient light blocking as taught by Adachi et al.

Sealants were conventionally put on alignment layers, avoiding unnecessary processing to remove them in the areas where the light blocking layers are form. The references to Kondo and Nishiguchi et al evidence this. Therefore it would have been obvious, in the devices of Misawa as modified above (or Lebrun for the reversed situation), to put the sealant above the alignment layers to avoid having to remove them.

Claims 5, 7, 15 and 21 are a display device according to claim 1 wherein the substrates are bonded each other with the sealing member and a device according to claim 1 further comprising a liquid crystal material between the substrates, wherein the sealing member seals the liquid crystal material and claim 15 is a device according claim 8 further comprising liquid crystal material injected between the first and the second substrate. Claim 21 is a device according claim 16 further comprising a liquid crystal material injected between the first substrate and the second substrate. These are met by Misawa as modified by Lebrun as the Misawa is modified to include the light blocking seal of Lebrun which provides these functions. Claims 10 and 18 are a device according to claim 8 wherein said shift register circuit comprises least a clocked inverter and inverter. As the shift register is part of the OR, so is met by the buffer whether or not this claim language is met. Regarding claim 14 which is an electronic device according to claim 8 wherein said device is a projector, the projector is explicitly taught by the Misawa. Claim 3 is a display device according claim 1 wherein one of an electrode or a wiring line connected to a source or drain of a thin-film transistor formed in the matrix circuit is one of a metal film, a

semiconductor film, and a silicide film, and wherein a light blocking film for the thin-film transistor is formed by using the one the of the metal film, the semiconductor film, and a silicide film. This is met by the combined references as the secondary reference places a light blocking film over all of the elements of the driver circuit.

Claim 4 is a display device according to claim 1 wherein said pair of the substrates are glass substrates or quartz substrates. These were the conventionally used materials, and would have been obvious to one of ordinary skill for that reason.

Inverters were conventionally used as a fundamental building block required to build driving circuits, and so to the reason to use them was to use the use the established technology. Therefore it would have been obvious, in the device of the references above, to employ inverters as was conventionally used for the benefit of using the established technology.

Claims 2, 6, 7, 11 and 19, 23, 33-34, 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Misawa 5250931in view in view of Lebrun et al 5606194, Adachi et al, 5155612, Kondo 5625473 and Nishiguchi et al 5621553 as applied above, and further in view of Wakai 5003356.

Claims 2, 9 and 7 are a display device according claim 1 wherein active matrix circuit has pixels arranged in matrix form, and wherein regions in each of the pixels where source lines and drain lines overlap with a pixel electrode form a black matrix. Claim 9 is a device according to claim 8 wherein said device does

not include a black matrix. Claim 17 is a device according to claim 16 wherein said device does not include a black matrix. The use of the pixels overlapping the gate and source lines was a notoriously well known method of providing a low cost black matrix in liquid crystal devices. This is evidenced by Wakai . Therefore it would have been obvious to one of ordinary skill to overlap these for the benefit of the low cost.

Claims 6, 11 and 19 are a device according to claim 1 further comprising: at least CMOS transistor formed in the driver circuit region, said CMOS transistor having an n-channel thin film transistor and a p-channel thin transistor;a film transistor formed in each pixel in the active matrix circuit, said thin film transistor having at an active layer, to said active layer, a gate electrode adjacent to said gate insulating film, wherein light blocking film is formed said gate electrode. Claim 19 is substantially a device according to claim 16 wherein, said first p-channel thin film transistor comprises, first source region and a first drain region formed over said first substrate, a first channel forming region formed between said first region and source regions, a first gate insulating region formed adjacent to said source and drain regions and said first channel forming region, a first gate electrode formed adjacent to said first gate insulating film, said n-channel thin film transistor comprises, a third region and a third drain region formed over said first substrate, a third channel forming region formed between said third source and drain regions, a third gate insulating region formed adjacent to said third source and drain regions and said third channel forming region, a third gate electrode formed adjacent to said third gate insulating film, said second p-

channel thin film transistor comprises, second source region and a second drain region formed over said first substrate, a second channel forming region formed between second source and drain regions, second gate said second source and drain regions and second channel forming region second gate electrode formed adjacent said second gate insulating film, wherein a second gate electrode, with light blocking film is formed. Claim 11 is a device according claim 8 further comprising: at least a CMOS transistor formed in said driver circuit region, said CMOS transistor having an n-channel thin transistor and a p-channel thin transistor; a thin film transistor formed in said pixel, said thin film transistor having at least an active layer, a gate insulating film adjacent said active layer, a gate electrode adjacent to said gate insulating film, and further comprising a light blocking film formed over said gate electrode. It was well known to employ a light block as claimed to prevent light activation. This is evidenced by Wakai, which teaches such a structure for this benefit (figure 13 and related discussion). Therefore would have been obvious to one of ordinary skill to use a metal light block near the gate for the reasons taught by Wakai and well known in the art.

Sealants were conventionally put on alignment layers, avoiding unnecessary processing to remove them in the areas where the light blocking layers are form. The references to Kondo and Nishiguchi et al evidence this. Therefore it would have been obvious, in the devices of Misawa as modified above (or Lebrun for the reversed situation), to put the sealant above the alignment layers to avoid having to remove them.

Response to Arguments

Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth A Parker whose telephone number is 571-272-2298. The examiner can normally be reached on M-F 10:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on 571-272-2293. The fax

phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kenneth A Parker
Primary Examiner
Art Unit 2871

Notice of References Cited	Application/Control No. 09/651,310	Applicant(s)/Patent Under Reexamination YAMAZAKI, SHUNPEI	
	Examiner Kenneth A Parker	Art Unit 2871	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,854,663	12-1998	Oh et al.	349/42
	B	US-5,745,202	04-1998	Yamauchi et al.	349/110
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	JP 02139523 A	05-1990	Japan	SAITO et al.	G02F 01/1339
	O	JP 04285915 A	10-1992	Japan	TORIGOE, TSUNEMITSU	G02F 01/1339
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

PAT-NO: JP404285915A

DOCUMENT-IDENTIFIER: JP 04285915 A

TITLE: LIQUID CRYSTAL DISPLAY ELEMENT

PUBN-DATE: October 12, 1992

INVENTOR-INFORMATION:
NAME
TORIGOE, TSUNEMITSU

ASSIGNEE-INFORMATION:

NAME	COUNTRY
ALPS ELECTRIC CO LTD	N/A

APPL-NO: JP03119552

APPL-DATE: March 14, 1991

INT-CL (IPC): G02F001/1339

US-CL-CURRENT: 349/153, 349/155

ABSTRACT:

PURPOSE: To surely prevent the light leakage from a sealing material without adversely affecting the printability of a sealing material and the orientation of a liquid crystal by adding a specific amt. of carbon powder into the sealing material and adding a specific amt. of black spacers thereto.

CONSTITUTION: An epoxy resin 6 as a thermosetting resin added with the carbon powder 7 and the black spacers 8 is used as the sealing material 3 which is provided between an upper electrode substrate 1 and a lower electrode

substrate 2 of the liquid crystal display element and is used to adhere these electrode substrates 1, 2. The carbon powder 7 is added at 0.5 to 1.0wt.% to this sealing material and the black spacers having the grain size slightly smaller than the gap between the two electrode substrate s 1, 2 is added at 5 to 10wt.% thereto. The black spacers 5 are formed by coating the surfaces of spherical divinyl benzene resins 8a with a coloring material 8b. The light transparency of the sealing material 3 is drastically lowered in this way without impairing the printability.

(19)日本国特許庁（ＪＰ）　(12) **公開特許公報（A）**　(11)特許出願公開番号

特開平4－285915

(43)公開日　平成４年(1992)10月12日

(51)Int.Cl.[5]	識別記号	庁内整理番号	ＦＩ	技術表示箇所
Ｇ０２Ｆ　1/1339	５００	7724－2K		

審査請求　未請求　請求項の数１(全　３　頁)

(21)出願番号　特願平3－119552

(22)出願日　平成３年(1991)３月14日

(71)出願人　000010098
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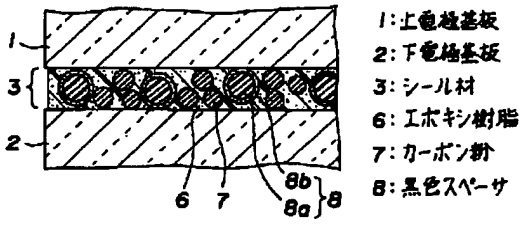
(74)代理人　弁理士　武　顕次郎

(54)【発明の名称】　液晶表示素子

(57)【要約】
【目的】　ＬＣＤのシール材中に添加するカーボン粉の量を抑えつつ該シール材の遮光性を高めることにより、シール材の印刷性や液晶の配向に悪影響を及ぼすことなく該シール材からの光洩れを確実に防止できるようにする。
【構成】　シール材３中に、カーボン粉７を０．５～１．０重量％添加するとともに、粒径が両電極基板１，２間のギャップ以下で黒色を呈する黒色スペーサ８を５～１０重量％添加した。

【図１】



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【特許請求の範囲】

【請求項1】　シール材を介して積層・接着された2枚の電極基板の間に液晶を封入してなり、両電極基板間に電圧を印加することにより表示パターンを照光せしめる液晶表示素子において、上記シール材中に、カーボン粉が0．5～1．0重量%添加してあるとともに、粒径が上記両電極基板間のギヤツプ以下で黒色を呈する黒色スペーサが5～10重量%添加してあることを特徴とする液晶表示素子。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は、2枚の電極基板間に電圧を印加することにより表示パターンを照光せしめるネガ表示タイプの液晶表示素子（以下、ＬＣＤと略称）に係り、特にそのシール材に関する。

【0002】

【従来の技術】この種のＬＣＤは図3に示す如く、ガラス板等に透明電極をパターニングしてなる上電極基板1および下電極基板2と、両電極基板1，2の対向面の周縁部どうしを接着しているシール材3と、両電極基板1，2の間でシール材3の内側に封入された液晶4とによつて基本的に構成されており、電圧無印加時にはこのＬＣＤの全面でバツクライト5は透過不能であるが、両電極基板1，2の電極パターン間に所定の電圧を印加すると、その部分でバツクライト5がＬＣＤを透過するので、電極パターンに対応した表示パターンが照光されるようになつている。そして、上記シール材3としては一般に、エポキシ樹脂等の熱硬化性樹脂が用いられ、これを上電極基板1もしくは下電極基板2に帯状に印刷した後、両電極基板1，2を重ね合わせて加圧・加熱することにより、これら両電極基板1，2が所定のギヤツプを保つて積層・接着され、そこに液晶4を封入してＬＣＤが製造される。なお、かかるＬＣＤのギヤツプ（セルギヤツプ）は、両電極基板1，2間に多数個介在させてあるガラススペーサや樹脂スペーサの粒径によつて規定される。

【0003】ところで、このようなネガ表示タイプのＬＣＤにあつては、電圧が印加される個所以外での光洩れを確実に防止しなければならないが、実際には、乳白色を呈するシール材3が10%程度の光透過率を有するため、このシール材3からの光洩れが表示品位を著しく損なう要因となつていた。

【0004】そこで従来、特開昭61－215525号公報に開示されている如く、予めシール材中にカーボン粉を添加しておくことで、その光透過率を大幅に減じるという提案がなされている。

【0005】

【発明が解決しようとする課題】しかしながら上記従来提案は、カーボン粉の凝集によりシール材中に空洞が生じてしまうので、この空洞部分で光洩れを起こしやすく、これを回避するためにカーボン粉の添加量を増やすと、シール材の印刷性が極端に悪くなるという不具合があつた。また、シール材中にカーボン粉が多く添加されている場合、該シール材の近傍で液晶の配向不良が惹起される可能性があるので、信頼性を損なう要因となつていた。

【0006】本発明はこのような事情に鑑みてなされたもので、その目的は、シール材の印刷性や液晶の配向に悪影響を及ぼすことなく該シール材からの光洩れを確実に防止できるネガ表示タイプのＬＣＤを提供することにある。

【0007】

【課題を解決するための手段】上記した本発明の目的は、シール材中に、カーボン粉を0．5～1．0重量%添加するとともに、粒径が両電極基板間のギヤツプ以下で黒色を呈する黒色スペーサを5～10重量%添加することによつて達成される。

【0008】

【作用】カーボン粉の添加量が1重量%以下で、かつ黒色スペーサの添加量が10重量%以下であれば、シール材の印刷性や液晶の配向にほとんど影響を及ぼさず、また、カーボン粉の凝集によつて生じる空洞に黒色スペーサが入り込んでいくので、光洩れの原因となる該空洞が少なくなつてシール材の遮光性が高まる。

【0009】

【実施例】以下、本発明の実施例を図に基づいて説明する。

【0010】本実施例では図1に示す如く、ＬＣＤの上電極基板1と下電極基板2との間に介設されて両電極基板1，2を接着するシール材3として、熱硬化性樹脂としてのエポキシ樹脂6にカーボン粉7と黒色スペーサ8とを添加したものを用いた。ここで、黒色スペーサ8は、球状のジビニルベンゼン樹脂8ａの表面に着色剤8ｂを塗布したもので、この着色剤8ｂは、アントラキノン系の青の色素とアゾ系の赤紫の色素とアゾ系の黄の色素との等分混合体である。また、この黒色スペーサ8の粒径は6μmで、両電極基板1，2間のギヤツプ（セルギヤツプ）6．5μmよりも若干小さく設定されている。

【0011】そして、カーボン粉や黒色スペーサの添加量が異なる複数種類のシール材について、それぞれＬＣＤを作製し、当該シール材を透過する光の透過率を測定した。図2は、カーボン粉を1重量%添加し、黒色スペーサを0～10重量%添加した場合の測定結果を示している。なお、図2中の測定値Ａは比較例で、カーボン粉と黒色スペーサのいずれをも添加しなかつた場合の測定結果である。

【0012】上記測定結果ならびにシール材の印刷性を評価すると、まず、カーボン粉については、その添加量が1重量%を越えると印刷性が劣化し始め、添加量が

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0．5重量%より少ないと光透過率を十分に低減させることができなかつた。また、黒色スペーサについては、添加量が10重量%を越えると印刷性が劣化し始めるものの、図2にも示すようにカーボン粉と併用した場合、添加量が5重量%以上で光透過率を1%以下に低減することができた。

【0013】したがつて、カーボン粉を0．5～1．0重量%添加するとともに、黒色スペーサを5～10重量%添加することにより、印刷性を損なうことなくシール材の光透過率を激減させ、該シール材からの光洩れを確実に防止することができる。このようにカーボン粉と黒色スペーサとの併用でシール材の遮光性が著しく高まるのは、カーボン粉の凝集によつて生じる空洞に黒色スペーサが入り込むためであると考えられる。また、カーボン粉の添加量が1重量%以下であることからシール材近傍で配向不良を惹起する虞れがなく、よつて印刷性のみならず信頼性も損なわれないという利点がある。

【0014】

【発明の効果】以上説明したように本発明によれば、シール材中にカーボン粉と黒色スペーサとを適量添加する

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ことで該シール材からの光洩れを確実に防止することができ、しかもカーボン粉の添加量が少ないのでシール材の印刷性や液晶の配向への悪影響が回避でき、よつて生産性や信頼性に支障をきたすことなくネガ表示タイプのLCDの表示品位を高めることができる。

【図面の簡単な説明】

【図1】本発明の実施例を説明するための要部断面図である。

【図2】本発明の実施例に係る黒色スペーサの添加量とシール材の光透過率との関係を示す特性図である。

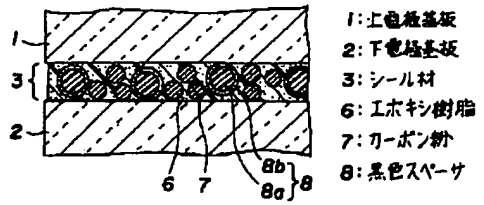
【図3】LCDの基本構成を説明するための断面図である。

【符号の説明】

1　上電極基板
2　下電極基板
3　シール材
6　エポキシ樹脂
7　カーボン粉
8　黒色スペーサ

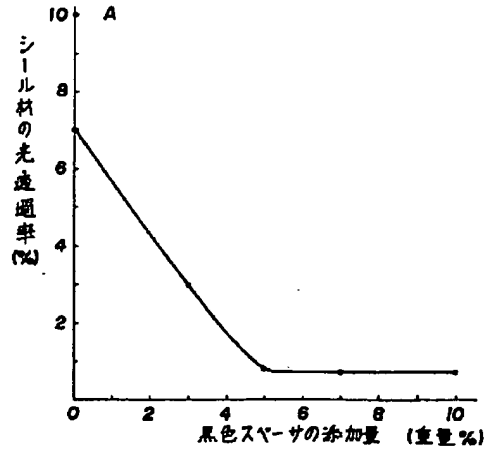
【図1】

【図1】



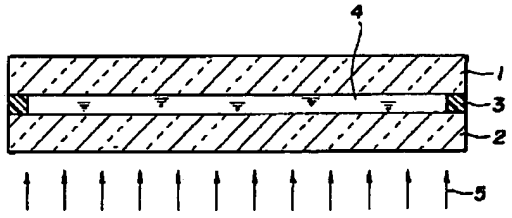
【図2】

【図2】



【図3】

【図3】



PAT-NO: JP402139523A

DOCUMENT-IDENTIFIER: JP 02139523 A

TITLE: LIQUID CRYSTAL DISPLAY ELEMENT

PUBN-DATE: May 29, 1990

INVENTOR-INFORMATION:
NAME
SAITO, TAKESHI
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ASSIGNEE-INFORMATION:

NAME	COUNTRY
HITACHI LTD	N/A

APPL-NO: JP63292298

APPL-DATE: November 21, 1988

INT-CL (IPC): G02F001/1339

US-CL-CURRENT: 349/153

ABSTRACT:

PURPOSE: To improve the position accuracy of a display part and to decrease the man-hours for operation and material cost by forming a sealing material to a black or nearly black color.

CONSTITUTION: An upper glass substrate 1 formed with an upper electrode 1a and a lower glass substrate 2 formed with a lower electrode 2a are disposed to face each other and the circumference thereof is sealed by the sealing material 3. The sealing material 3 is formed by incorporating a dye

of a black or
nearly black color into the sealing material. An upper polarizing plate 5 and
a lower polarizing plate 6 are stuck to the outer side of the substrates 1, 2.
The sealing material 3 absorbs and shuts off light and the display region of a
bright contour is obtd.

⑲日本国特許庁(JP)　⑪特許出願公開

⑫公開特許公報(A)　平2−139523

⑤Int. Cl.⁵	識別記号	庁内整理番号	㊸公開　平成2年(1990)5月29日
G 02 F 1/1339	505	7370−2H	

審査請求　未請求　請求項の数 1　(全2頁)

㊹発明の名称　液晶表示素子

㉑特　願　昭63−292298
㉒出　願　昭63(1988)11月21日

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㉔代理人　弁理士　小川　勝男　外1名

明　細　書

1．発明の名称

液晶表示素子

2．特許請求の範囲

1．対向配置した2枚のガラス基板の周囲をシール材でシールし、内部に液晶を封入してなる液晶表示素子において、前記シール材は、黒色または黒色に近い色よりなることを特徴とする液晶表示素子。

3．発明の詳細な説明

〔産業上の利用分野〕

本発明は液晶表示素子に係り、特に表示領域を引き立て鮮明な表示を行うための液晶表示素子構造に関する。

〔従来の技術〕

従来、液晶表示素子において、表示領域を引き立て鮮明な表示を行うためには、例えば実開昭50−68679号に示すように、表示面にカバーを付け表示面以外の所を覆つている。

〔発明が解決しようとする課題〕

上記従来技術は、表示面以外の所を覆うようにカバーを設けてなるので、カバーの位置ずれによつて必要な部分まで覆つてしまつたり、またカバー材料の分、コスト高になるなどの問題があつた。

本発明の目的は、表示部の位置精度の向上、作業工数及び材料費の低減が図れる液晶表示素子を提供することにある。

〔課題を解決するための手段〕

上記目的は、2枚のガラス基板をシールするシール材を黒色または黒色に近い色にすることにより達成される。

〔作用〕

シール材は黒色よりなるので、光を吸収遮断する。これによつて、輪郭の鮮明な表示領域が得られる。

〔実施例〕

以下、本発明の一実施例を図により説明する。上電極1aが形成された上ガラス基板1と下電極2aが形成された下ガラス基板2とは、電極1a、2a面を対向させ、周囲をシール材3でシールし

て上下ガラス基板１、２の間隔を５～１０μmに保つている。ここで、前記シール材３は、シール材料に黒色または黒色に近い色の染料を混入したものよりなつている。そして、上下ガラス基板１、２の内部には液晶４が封入され、また上下ガラス基板１、２の外側には上偏向板５及び下偏向板６が貼付けられている。

このように、シール材３は黒色または黒色に近い色よりなるので、光を吸収遮断する。これによつて、輪郭の鮮明な表示領域が得られる。またシール材３はスクリーン印刷等で印刷塗布することにより、シールと同時に遮光マスクが完成するので、位置精度が向上すると共に、作業工数及び材料費が低減する。

〔発明の効果〕

本発明によれば、シール材が黒色または黒色に近い色よりなるので、表示領域の輪郭の位置精度が向上すると共に、作業工数及び材料費が低減する。

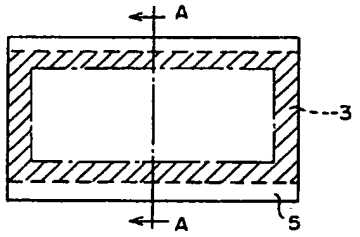
4．図面の簡単な説明

図は本発明の一実施例を示し、第１図は正面図、第２図は第１図のＡ－Ａ線断面図である。

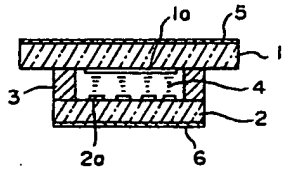
１…上ガラス基板、　２…下ガラス基板、
３…シール材、　４…液晶。

代理人　弁理士　小　川　勝　男

第　１　図



第　２　図



1：上ガラス基板
2：下ガラス基板
3：シール材
4：液晶

AMLCD MODELING AND DISPLAY PERFORMANCE AT IMAGE QUEST TECHNOLOGIES

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Fremont, CA 94539

ABSTRACT

Avionic cockpit display applications require AMLCD's having extended and specific viewing angle characteristics. A typical cone is +/-60 degrees horizontal, and 0 to +30 degrees vertical. We used a Berreman 4x4 matrix based model to identify the necessary birefringent film values to optimize the display. The key parameter in the model was maximizing the region where the contrast ratio is greater than 50:1, without distorting the color gamut. We will show how well our current production units match our modeling results.

INTRODUCTION

Active matrix liquid crystal displays (AMLCD's) are finding increasing use in avionic cockpit applications. The requirements [1] for avionic displays are, however, quite different and more stringent than those for commercial displays. This includes the viewing angle requirements. Unlike commercial displays, avionic displays must often be viewed by both pilot and copilot. Thus they require a very wide horizontal field of view. Further, it is typically not possible to tilt the display in the aircraft towards the operator. Hence, an off axis vertical viewing cone is mandated. Naturally, the field of views differ greatly depending upon where the display is placed, and upon the type of aircraft. However, a generic set of requirements can be assembled which can serve as a goal for modeling efforts. The model that matches these requirements then becomes the standard display configuration, which we can adjust to meet different customer needs.

MODELING RESULTS

In this work we used the modeling program Twist Cell Optics [2] from Kent State University which is based on the fast Berreman 4x4 matrix method. Based on several potential customers requirements we generated the following model goals:

Field of View (FOV)		
	Horizontal	+/- 60 degrees
	Vertical	0, + 30 degrees
Contrast Ratio		
	> 20:1	within defined FOV
		(maximize >50:1 region)
Chromaticity		
	$\Delta r < 0.02$	for colors within FOV
	$\Delta C^* < 24$	for black state within FOV

No contrast inversion within FOV.

With a few modifications, these requirements would satisfy our current contracts. The chromatic shift Δr above is defined as

$$\Delta r = \sqrt{(u'-u'_o)^2 + (v'-v'_o)^2}$$

where u' and v' are the CIE 1976 chromaticity coordinates and u'_o and v'_o are the chromaticity

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